Xynergy^{BF}

Versatile System-on-Module with Blackfin BF537, Spartan-6 FPGA, 128MB DDR3, 10/100 Ethernet, CAN, UART, USB, I²C, ADC/DAC

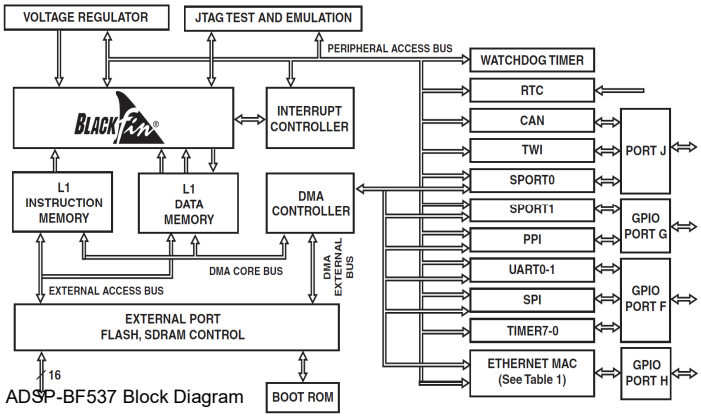
Xynergy^{BF} combines Analog Devices' Blackfin ADSP-BF537 with a Xilinx Spartan-6 FPGA and a large amount of DDR3 memory for high-performance digital signal processing.

The Blackfin's external memory interface is directly connected to the FPGA ensuring high-speed data transfers between the two devices.

The Blackfin can be clocked at up to 600 MHz and has 132 KB of on-chip single-cycle SRAM. The 64M x 16 DDR-3 memory, which is connected to the FPGA, can be accessed by the Blackfin page-wise via its memory bus, allowing the Blackfin to use it as external bulk memory.

The Blackfin provides numerous communications interfaces, including 10/100 Ethernet with PHY, USB (via MCP2221A), CAN, a UART (RX/TX only), I²C, and up to 21 general purpose I/O lines.

A 4-channel serial ADC (12 bit, 500 ksps) and a 2-channel 12-bit serial DAC simplify signal acquisition and processing. All interface signals are available at the 200-pin SO-DIMM edge connector.



ADSP-BF537 Block Diagram

The FPGA expands I/O capabilities of the **Xynergy^{BF537}** by delivering up to 34 differential (LVDS) I/O lines plus two LCDS clocks, useful for connecting FMC compliant expansion boards, and four single-ended general purpose I/O lines.

For the pinout of the SO-DIMM connector, please refer to: downloads.dsp-sys.de/XynergyBF537/Pinout.pdf

A break-out board with special function connectors and many pins accessible at 100mil header plus JTAG headers is also available.

The module is supported by Analog Devices VisualDSP and CrossCore tools. For the FPGA, Xilinx ISE 14.7 (free for download at www.xilinx.com) is required.

More information on this product can be found at www.dsp-sys.de/BF

Specifications:

Power consumption: 2 Watts*) @ 3.3V (alternate V_{IO} for the FPGA is 2.5V (Bank 0 & 2))

Processor: Blackfin ADSP-BF537 in BGA182 package

FPGA: Spartan-6 XC6SLX16 (XC6SLX45 optional)

External Memory: 128 MB DDR3, 128 Mb SPI flash

Digital I/O: Up to 111 general purpose I/O pins (34 LVDS pairs)

Analog: ADC124S051 (4-ch ADC) & AD5623R (2-ch DAC)

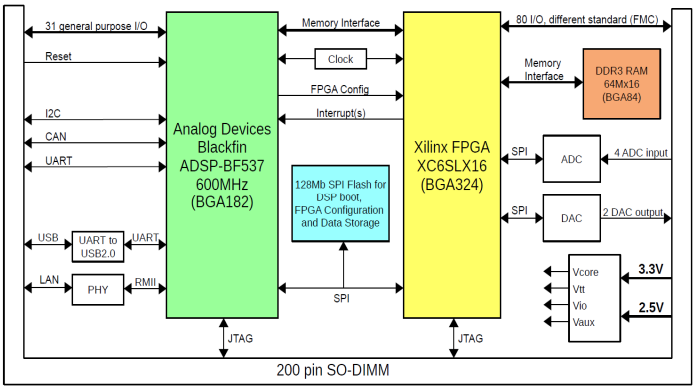
Physical Dimensions: 67.6 x 31.8 x 6mm (SO-DIMM200)

Weight: approx. 6grams

Matching Socket: e.g., TE Connectivity 1473005-4

Bottom/Top Component Height: 2.0/2.0mm (max.)

**) depending on the application*



Simplified Xynergy^{BF537} Block Diagram

Development Tools

Blackfin: VisualDSP 5.x or CrossCore tool chains

FPGA: Xilinx ISE Design Suite 14.7

Typical applications:

Industrial Control, Industrial Imaging, Motion Control, M2M Communication, High Performance Computing, Modems, etc.

A.R. Bayer DSP Systeme GmbH
Vohwinkelallee 8
40229 Düsseldorf / Germany
Phone: +49-211-271 46 30
Fax: +49-211-210 81 76
Email: gmbh@dsp-sys.de
Web: https://dsp-sys.de